1. An apparatus for correcting a call/return stack in a pipelined microprocessor, the apparatus comprising:

a first stack, comprising a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline;

a second stack, coupled to said first stack, comprising a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline; and

control logic, coupled to said first and second stacks, for receiving a control signal indicating a call or return instruction is passing from said first plurality of stages to said second plurality of stages, wherein said control logic moves said correction information associated with said call or return instruction from said first stack to said second stack in response to said control signal.

2. The apparatus of claim 1, wherein said control logic moving said correction information associated with said call or return instruction from said first stack to said second stack comprises said control logic removing said correction information from a bottom valid one of said first plurality of entries in said first stack and pushing said removed correction information onto said second stack.

3. The apparatus of claim 2, wherein said control logic removing said correction information from said bottom valid one of said first plurality of entries in said first stack comprises invalidating said bottom valid one of said first plurality of entries in said first stack.

4. The apparatus of claim 1, wherein if said related call or return instruction is a call instruction, said correction information comprises a command to pop a return address off the internal call/return stack.

5. The apparatus of claim 1, further comprising:

a third stack, coupled to said control logic, comprising a third plurality of entries for storing return addresses related to call instructions present in said first or second plurality of pipeline stages.

6. The apparatus of claim 5, wherein if said related call or return instruction is a return instruction, said correction information comprises a command to pop a return address off said third stack and push said return address onto the internal call/return stack.

7. The apparatus of claim 1, further comprising:

a plurality of valid bits, coupled to said first stack, for specifying whether corresponding ones of said first plurality of entries are valid.

8. The apparatus of claim 1, further comprising:

a plurality of valid bits, coupled to said second stack, for specifying whether corresponding ones of said second plurality of entries are valid.

9. The apparatus of claim 1, wherein said control signal indicates said call or return instruction has reached a bottom stage of said first plurality of pipeline stages.

10. The apparatus of claim 9, wherein said control signal indicates said bottom stage of said first plurality of pipeline stages is not stalled.

11. The apparatus of claim 10, wherein said control signal indicates a branch instruction preceding said call or return instruction has not been detected as mispredicted by the microprocessor.

12. The apparatus of claim 1, further comprising:

a second control signal, received by said control logic, for indicating said call or return instructions present in said first plurality of pipeline stages were speculatively incorrectly executed.

13. The apparatus of claim 12, wherein said second control signal indicates a branch instruction preceding said call or return instructions present in said first plurality of pipeline stages was mispredicted by the microprocessor.

14. The apparatus of claim 12, wherein said second control signal indicates one of said call or return instructions present in said first plurality of pipeline stages was mispredicted by the microprocessor.

15. The apparatus of claim 12, wherein said second control signal is generated by a bottom stage of said first plurality of pipeline stages.

16. The apparatus of claim 12, wherein said control logic corrects the call/return stack using said correction information stored in said first plurality of entries of said first stack, in response to said second control signal.

17. The apparatus of claim 16, wherein for each valid one of said first plurality of entries, said control logic pops a top said valid one of said first plurality of entries from said first stack, and corrects the call/return stack based on said correction information stored therein.

18. The apparatus of claim 16, further comprising:

a third control signal, received by said control logic, for indicating said call or return instructions present in said first and second plurality of pipeline stages were speculatively incorrectly executed.

19. The apparatus of claim 18, wherein said third control signal indicates a branch instruction preceding said call or return instructions present in said first and second plurality of pipeline stages was mispredicted by the microprocessor.

20. The apparatus of claim 18, wherein said third control signal indicates an instruction preceding said call or return instructions present in said first and second plurality of pipeline stages generated a microprocessor exception.

21. The apparatus of claim 18, wherein said third control signal indicates one of said call or return instructions present in said first and second plurality of pipeline stages was mispredicted by the microprocessor.

22. The apparatus of claim 18, wherein said third control signal is generated by a bottom stage of said second plurality of pipeline stages.

23. The apparatus of claim 18, wherein said control logic corrects the call/return stack using said correction information stored in said first and second plurality of entries of said first and second stacks, in response to said third control signal.

24. The apparatus of claim 23, wherein for each valid one of said first plurality of entries, said control logic pops a top said valid one of said first plurality of entries from said first stack, and corrects the call/return stack based on said correction information stored therein, then for each valid one of said second plurality of entries, said control logic pops a top said valid one of said second plurality of entries from said second stack.

25. The apparatus of claim 1, further comprising:

a second signal, received by said control logic, for indicating one of said call or return instructions present in said second plurality of stages of the microprocessor pipeline is no longer speculative, wherein said control logic updates said second stack in response to said second signal.

26. The apparatus of claim 25, wherein said control logic updating said second stack in response to said second signal comprises invalidating one of said second plurality of entries storing said correction information for said no longer speculative one of said call or return instructions.

27. The apparatus of claim 26, wherein said invalidating one of said second plurality of entries storing said correction information for said no longer speculative one of said call or return instructions comprises invalidating a bottom valid one of said second plurality of entries.

28. The apparatus of claim 1, further comprising:

a second signal, received by said control logic, for requesting the call/return stack be updated in response to the presence of one of said call or return instructions in said first plurality of pipeline stages, wherein said control logic stores correction information related to said one of said call or return instructions into said first stack in response to said second signal.

29. The apparatus of claim 28, wherein said control logic storing said correction information related to said one of said call or return instructions into said first stack comprises said control logic pushing said correction information onto said first stack.

30. A pipelined microprocessor, comprising:

a call/return stack (CRS);

first and second pipeline stages, for generating a true value on first and second signals, respectively, in response to detection of a misprediction of a branch instruction present in said first and second pipeline stage, respectively, wherein said first stage is above said second stage in the pipeline;

an apparatus, coupled to receive said first and second signals, for maintaining first information related to call or return instructions present in stages of the pipeline above said first stage, and for maintaining second information related to call or return instructions present in stages of the pipeline between said first and second stages, wherein said apparatus is configured to selectively correct said CRS using said first information if said first signal is true, or said first and second information if said second signal is true.

31. The microprocessor of claim 30, further comprising:

a third signal, received by said apparatus, for indicating one of said call or return instructions has arrived in said first stage;

wherein said apparatus transfers to said second information a portion of said first information related to said one of said call or return instructions, in response to said third signal.

32. The microprocessor of claim 30, further comprising:

a third signal, received by said apparatus, for indicating one of said call or return instructions has arrived in said second stage;

wherein said apparatus removes from said second information a portion of said second information related to said one of said call or return instructions arrived in said second stage, in response to said third signal.

33. The microprocessor of claim 30, further comprising:

a third signal, received by said apparatus, for indicating detection of an exception generated by an instruction present in said second pipeline stage;

wherein said apparatus corrects said CRS using said first and second information if said third signal is true.

34. A method for maintaining consistency between a call/return stack (CRS) in a pipelined microprocessor and a memory coupled thereto, the method comprising:

receiving requests to update the CRS in response to a presence of call or return instructions;

storing correction information into a first buffer, in response to said receiving;

detecting a condition in which one of the call or return instructions has proceeded past a first stage of the microprocessor pipeline configured to detect an invalidating event, after said storing; and

moving a portion of the correction information from the first buffer to a second buffer, in response to said detecting.

35. The method of claim 34, wherein said invalidating event comprises a branch instruction misprediction.

36. The method of claim 34, further comprising:

correcting the CRS with the correction information stored in the first buffer if the first stage detects the invalidating event.

37. The method of claim 36, further comprising:

correcting the CRS with the correction information stored in the first and second buffer if a second stage of the microprocessor pipeline detects a second invalidating event, wherein the second stage is below the first stage.

38. The method of claim 37, wherein said invalidating event comprises a branch instruction misprediction.

39. The method of claim 37, wherein said invalidating event comprises an exception.

40. A computer data signal embodied in a transmission medium, comprising:

computer-readable program code for providing an apparatus for correcting a call/return stack in a pipelined microprocessor, said program code comprising:

first program code for providing a first stack, comprising a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline;

second program code for providing a second stack, coupled to said first stack, comprising a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline; and

third program code for providing control logic, coupled to said first and second stacks, for receiving a control signal indicating a call or return instruction is passing from said first plurality of stages to said second plurality of stages, wherein said control logic moves said correction information associated with said call or return instruction from said first stack to said second stack in response to said control signal.